

SRAM NV Controller With Reset

Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3-volt primary cell input
- 3-volt rechargeable battery input/output
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

General Description

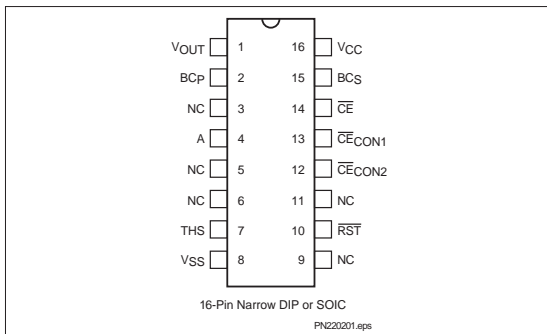
The CMOS bq2202 SRAM Nonvolatile Controller With Reset provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V_{CC} input for an out-of-tolerance condition. When out-of-tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V_{CC} supply to the battery-backup supply as V_{CC} decays. On a subsequent power-up, the V_{OUT} supply is automatically switched from the backup supply to the V_{CC} supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

Pin Connections



Pin Names

V_{OUT}	Supply output
\overline{RST}	Reset output
THS	Threshold select input
\overline{CE}	Chip enable active low input
\overline{CE}_{CON1} , \overline{CE}_{CON2}	Conditioned chip enable outputs
A	Bank select input
BCP	3V backup supply input
BCS	3V rechargeable backup supply input/output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Functional Description

Two banks of CMOS static RAM can be battery-backed using the V_{OUT} and conditioned chip-enable output pins from the bq2202. As the voltage input V_{CC} slews down during a power failure, the two conditioned chip enable outputs, \overline{CE}_{CON1} and \overline{CE}_{CON2} , are forced inactive independent of the chip enable input \overline{CE} .

This activity unconditionally write-protects external SRAM as V_{CC} falls to an out-of-tolerance threshold V_{PF} . V_{PF} is selected by the threshold select input pin, THS. If THS is tied to V_{SS} , the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to V_{CC} , power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V_{SS} or V_{CC} for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT} (150 μ sec maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

bq2202

As the supply continues to fall past V_{PFD} , an internal switching device forces V_{OUT} to the internal backup energy source. $\overline{CECON1}$ and $\overline{CECON2}$ are held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the 5V supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT} . Outputs $\overline{CECON1}$ and $\overline{CECON2}$ are held inactive for time t_{CER} (120ms maximum) after the power supply has reached V_{PFD} , independent of the \overline{CE} input, to allow for processor stabilization.

During power-valid operation, the \overline{CE} input is passed through to one of the two \overline{CECON} outputs with a propagation delay of less than 10ns. The \overline{CE} input is output on one of the two \overline{CECON} output pins; depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output (\overline{RST}) goes active within t_{PFD} (150 μ sec maximum) after V_{PFD} , and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The \overline{RST} output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when \overline{RST} returns inactive.

Energy Cell Inputs—BCP, BCS

Two backup energy source inputs are provided on the bq2202—a primary cell BCP and a secondary cell BCS. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BCP pin should be grounded. The secondary cell input BCS is designed to accept constant-voltage current-limited rechargeable cells.

During normal 5V power valid operation, 3.3V is output on the BCS pin and is current-limited internally.

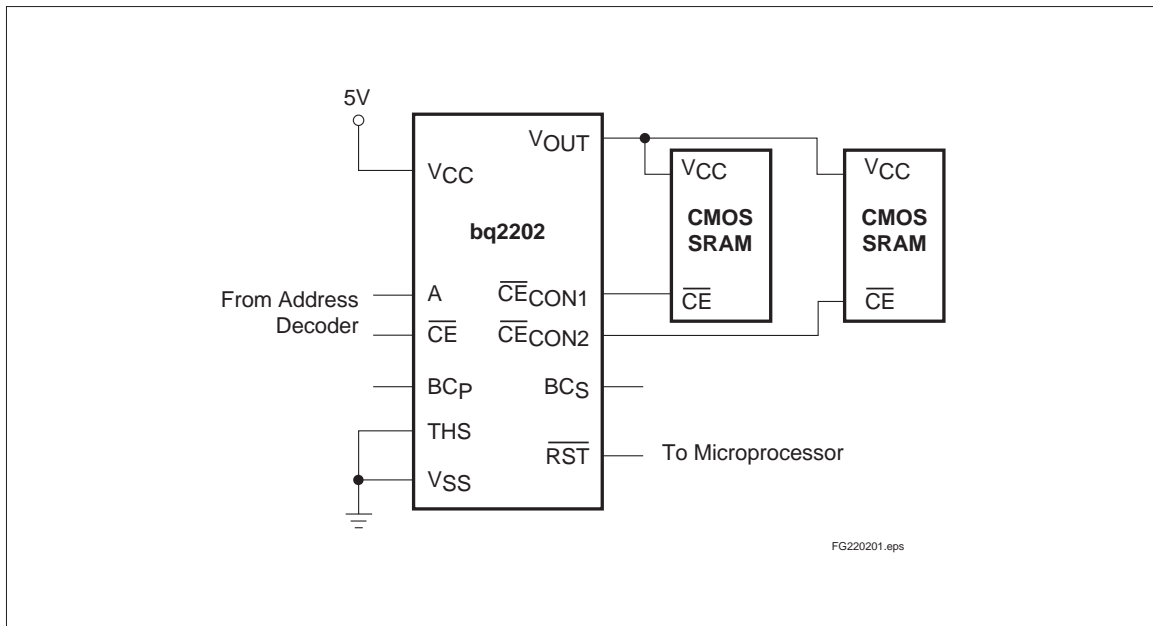


Figure 1. Hardware Hookup (5% Supply Operation)

If a secondary cell is not to be used, the BCS pin must be tied directly to VSS. If both inputs are used, during power failure the VOUT and CECON outputs are forced high by the secondary cell so long as it is greater than 2.5V. Only the secondary cell is loaded by the data retention current of the SRAM until the voltage at the BCS pin falls below 2.5V. When and if the voltage at BCS falls below 2.5V, an internal isolation switch automatically transfers the load from the secondary cell to the primary cell.

To prevent battery drain when there is no valid data to retain, VOUT, CECON1, and CECON2 are internally isolated from BCP and BCS by either:

- Initial connection of a battery to BCP or BCS or
- Presentation of an isolation signal on CE.

A valid isolation signal requires CE low as VCC crosses both VPF and VSO during a power-down. See Figure 2. Between these two points in time, CE must be brought to VCC * (0.48 to 0.52) and held for at least 700ns. The isolation signal is invalid if CE exceeds VCC * 0.54 at any point between VCC crossing VPF and VSO.

The battery is connected to VOUT, CECON1, and CECON2 immediately on subsequent application and removal of VCC.

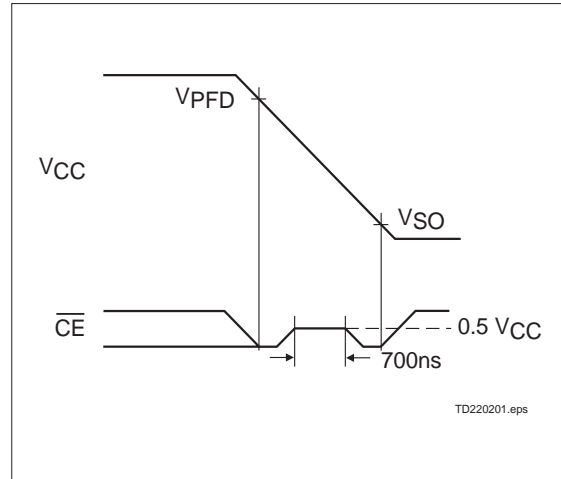


Figure 2. Battery Isolation Signal

Truth Table

Input		Output	
CE	A	CECON1	CECON2
H	X	H	H
L	L	L	H
L	H	H	L

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V _{CC}	DC voltage applied on V _{CC} relative to V _{SS}	-0.3 to +7.0	V	
V _T	DC voltage applied on any pin excluding V _{CC} relative to V _{SS}	-0.3 to +7.0	V	V _T ≤ V _{CC} + 0.3
T _{OPR}	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
T _{STG}	Storage temperature	-55 to +125	°C	
T _{BIAS}	Temperature under bias	-40 to +85	°C	
T _{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I _{OUT}	V _{OUT} current	200	mA	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = T_{OPR})

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V _{CC}	Supply voltage	4.75	5.0	5.5	V	THS = V _{SS}
		4.50	5.0	5.5	V	THS = V _{CC}
V _{BCP}	Backup cell input voltage	2.0	-	4.0	V	V _{CC} < V _{BC}
V _{BSC}		2.5	-	4.0		
V _{SS}	Supply voltage	0	0	0	V	
V _{IL}	Input low voltage	-0.3	-	0.8	V	
V _{IH}	Input high voltage	2.2	-	V _{CC} + 0.3	V	
THS	Threshold select	-0.3	-	V _{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC}.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
ILI	Input leakage current	-	-	± 1	μA	$V_{IN} = V_{SS}$ to V_{CC}
VOH	Output high voltage	2.4	-	-	V	$I_{OH} = -2.0mA$
VOHB	VOH, backup supply	$V_{BC} - 0.3$	-	-	V	$V_{BC} > V_{CC}$, $I_{OH} = -10\mu A$
VOL	Output low voltage	-	-	0.4	V	$I_{OL} = 4.0mA$
ICC	Operating supply current	-	3	6	mA	No load on V_{OUT} , \overline{CE}_{CON1} , and \overline{CE}_{CON2}
V _{PF} D	Power-fail detect voltage	4.55	4.62	4.75	V	$T_{HS} = V_{SS}$
		4.30	4.37	4.50	V	$T_{HS} = V_{CC}$
V _{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
IC _{CDR}	Data-retention mode current	-	-	100	nA	No load on V_{OUT} , \overline{CE}_{CON1} , and \overline{CE}_{CON2}
V _{OUT1}	V _{OUT} voltage	$V_{CC} - 0.2$	-	-	V	$V_{CC} > V_{BC}$, $I_{OUT} = 100mA$
		$V_{CC} - 0.3$	-	-	V	$V_{CC} > V_{BC}$, $I_{OUT} = 160mA$
V _{OUT2}	V _{OUT} voltage	$V_{BC} - 0.2$	-	-	V	$V_{CC} < V_{BC}$, $I_{OUT} = 100\mu A$
V _{BC}	Active backup cell voltage	-	V_{BCS}	-	V	$V_{BCS} > 2.5V$
		-	V_{BCP}	-	V	$V_{BCS} < 2.5V$
R _{BCS}	BC _S charge output internal resistance	500	1000	1750	Ω	$V_{BCSO} \geq 3.0V$
V _{BCSO}	BC _S charge output voltage	3.0	3.3	3.6	V	$V_{CC} > V_{PF}D$, \overline{RST} inactive, full charge or no load
I _{OUT1}	V _{OUT} current	-	-	160	mA	$V_{OUT} \geq V_{CC} - 0.3V$
I _{OUT2}	V _{OUT} current	-	100	-	μA	$V_{OUT} \geq V_{BC} - 0.2V$

Note: Typical values indicate operation at $T_A = 25^\circ C$, $V_{CC} = 5V$ or V_{BC} .

Capacitance ($T_A = 25^\circ C$, $F = 1MHz$, $V_{CC} = 5.0V$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
C _{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V
C _{OUT}	Output capacitance	-	-	10	pF	Output voltage = 0V

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)

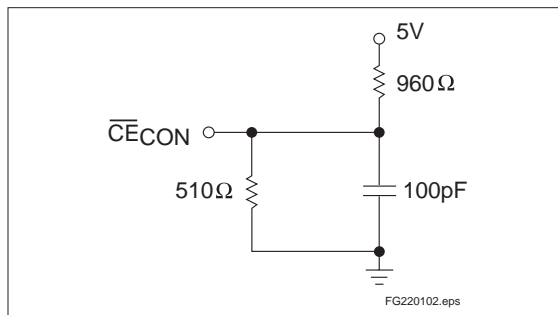


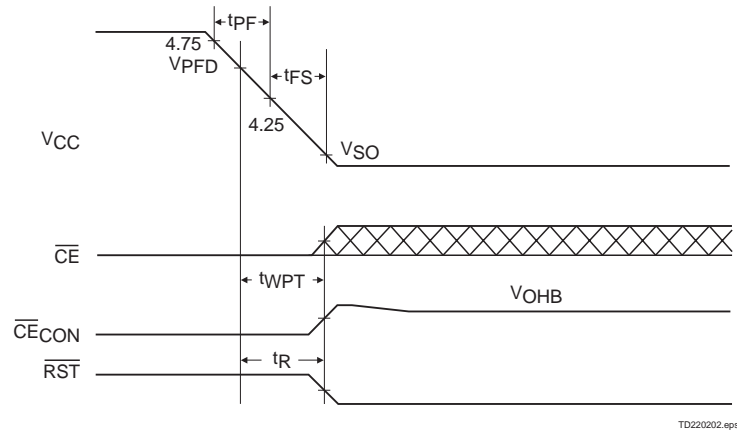
Figure 3. Output Load

Power-Fail Control (TA = TOPR)

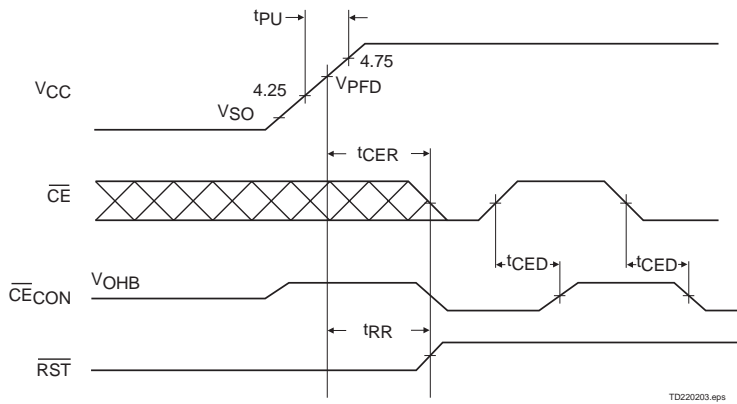
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tPF	VCC slew 4.75 to 4.25V	300	-	-	μs	
tFS	VCC slew 4.25 V to VSO	10	-	-	μs	
tPU	VCC slew 4.25 to 4.75V	0	-	-	μs	
tCED	Chip-enable propagation delay	-	7	10	ns	
tCER	Chip-enable recovery time	tRR	-	tRR	ms	Time during which SRAM is write-protected after VCC passes VPFDD on power-up
tRR	VPFD to $\overline{\text{RST}}$ inactive	40	80	120	ms	Time, after VCC becomes valid, before $\overline{\text{RST}}$ is cleared
tAS	Input A set up to $\overline{\text{CE}}$	0	-	-	ns	
tWPT	Write-protect time	tR	-	tR	μs	Delay after VCC slews down past VPFDD before SRAM is write-protected
tR	VPFD to $\overline{\text{RST}}$ active	40	100	150	μs	Delay after VCC slews down past VPFDD before $\overline{\text{RST}}$ is active

Note: Typical values indicate operation at TA = 25°C, VCC = 5V.

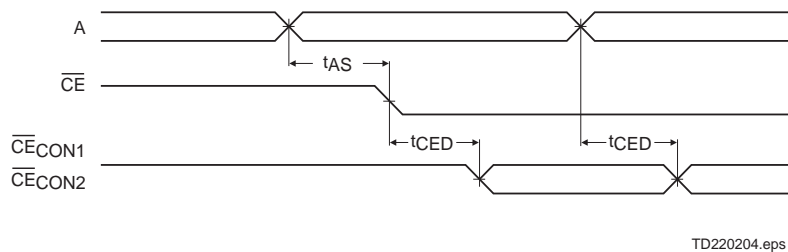
Power-Down Timing



Power-Up Timing

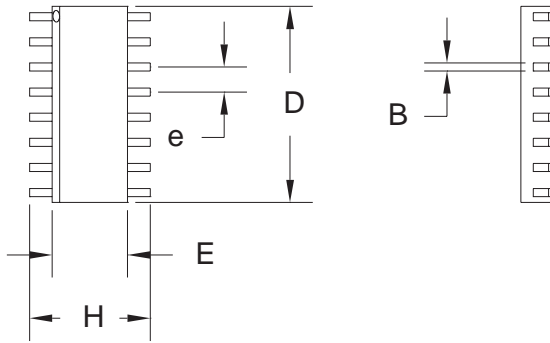


Address-Decode Timing



bq2202

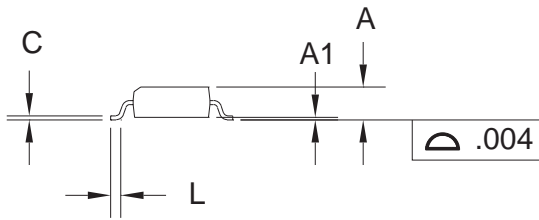
16-Pin SOIC Narrow



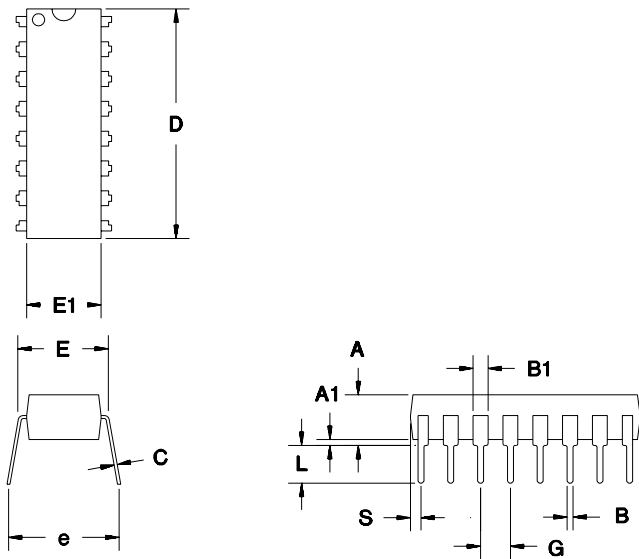
16-Pin SOIC Narrow (SN)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.



16-Pin DIP Narrow



16-Pin DIP Narrow (PN)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.740	0.770
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

All dimensions are in inches.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Deleted last sentence	Clarification
1	5	VBCSO—BCS charge output voltage	Was: 3.15 min, 3.3 typ, 3.45 max Is: 3.0 min, 3.3 typ, 3.6 max
2	5	Changed maximum charge output internal resistance (RBCS)	Was: 1500Ω Is: 1750Ω
3	1, 4, 5	10% supply operation	Was: THS tied to VOUT Is: THS tied to VCC

Note: Change 1 = Dec. 1992 B changes from Sept. 1991 A.
Change 2 = Nov. 1994 C changes from Dec. 1992 B.
Change 3 = Sept. 1997 D changes from Nov. 1994 C.

Ordering Information

bq2202

Temperature Range:

blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)

Package Option:

PN = 16-pin narrow plastic DIP
SN = 16-pin narrow SOIC

Device:

bq2202 SRAM Nonvolatile Controller With Reset

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
BQ2202PN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
BQ2202PN-N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
BQ2202SN	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
BQ2202SN-N	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
BQ2202SN-NTR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
BQ2202SNTR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265